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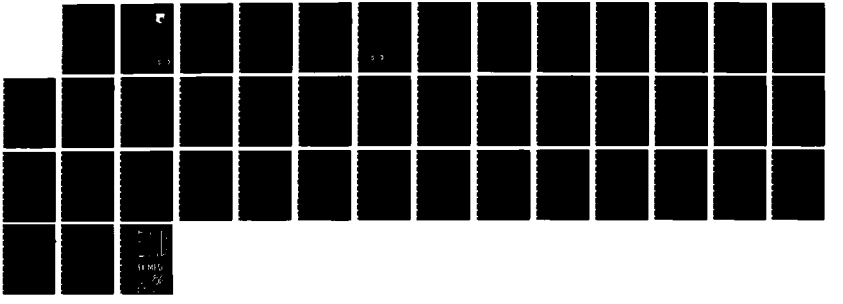

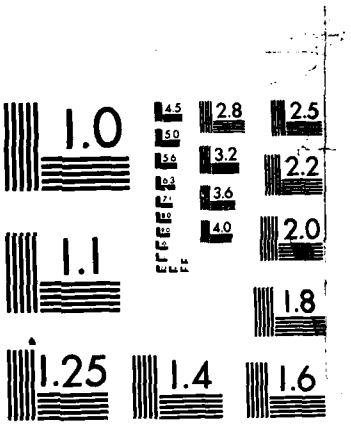

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EXAMINATION OF MILLIMETER-WAVE PERFORMANCE POTENTIAL OF MODULATION DOPED AlGaAs/GaAs FET STRUCTURES

Mukunda B. Das

Electronic Research Branch
Electronic Technology Division

September 1985

Final Report for Period 1 July 1983 - 30 June 1984

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This investigation involved a critical examination of the millimeter-wave performance requirements of the modulation-doped n-AlGaAs/GaAs FET structures. The results of this study revealed the need for a high aspect ratio design for the gate structure of MODFET's for millimeter-wave performance. A detailed design procedure has also been developed for submicron gate-length MODFET's, determination of carrier saturation velocity, and power gain and noise figure performance of MODFET's.

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TABLE OF CONTENTS

INTRODUCTION

Program Objective

As a Visiting Professor under the Air Force University Resident Research Program, the author was assigned to the ongoing efforts of the Air Force Wright Aeronautical Laboratories (AFWAL) efforts to bridge the gap between materials research and device development activities at AFWAL. Initial areas designated for the author's participation were (1) research in deep level and carrier transport measurements involving DLTS, PITS, gated Hall and magnetoresistance measurements, and (2) research on device measurements that show relationships between the materials parameters and device performance parameters.

When this assignment began the III-V compound research program at the AFWAL was being reoriented to investigate layered semiconductor structures initially with GaAs/AlGaAs hetero-structures. This area was considered having the potential of significant improvement in the device performance, as in the modulation-doped FET's, and the introduction of new physical concepts. The author's primary responsibilities under this new program included actual device characterization and performance evaluation and comparison with theoretical results and reported performances.

Selection of Research Elements

Preliminary organization revealed to the author a significant need to determine the high frequency potential of the emerging MODFET's (modulation-doped FET's). Thus, it was considered unwise to dilute this effort by pursuing research on deep levels in the AlGaAs/GaAs materials, as planned originally. The research elements selected for investigations are as follows:

(a) Understanding of the high-frequency potential of the emerging n-AlGaAs/GaAs MODFET's with submicron gate-lengths. This would include primarily the power gain limitations and gain/stability margin as they depend on structural and material details of the device.

(b) Characterize the carrier concentration and mobility as functions of gate applied voltage in the n-AlGaAs/GaAs MODFET structures and relate them with the carrier velocity saturation behavior in micron and submicron devices.

(c) Develop network models for the active and passive components in MODFET's and characterize practical devices based on these models.

(d) Carry out power gain and noise measurements on available short gate-length MODFET's and interpret the data in light of device models.

DESCRIPTION OF RESEARCH ACTIVITIES

Theoretical Investigation

A review of existing published literature (References 1-5) on high electron mobility transistors (HEMT's) -- which are also known as the modulation-doped FET's (MODFET's) or the two-dimensional electron gas FET's (TEGFET's) -- revealed the need to develop a useful MODFET d.c. model and a small-signal a.c. model. Starting with the charge-control concept, in line with that already in use for the conventional silicon MOSFET's, as introduced by Delagebeaudeuf and Linh (Reference 4), an attempt was made to combine the concept of current saturation due to carrier velocity saturation (Reference 6) in submicron gate-length MODFET's. This approach yielded a first order closed from D.C. and small-signal basic intrinsic device a.c. model for the MODFET based on the simplifying assumption that its gate capacitance is independent of the gate bias voltage. The extrinsic series resistance and parasitic capacitance effects and the output a.c. conductance, as present in practical devices, were also carefully incorporated in the overall a.c. network model that was developed for the MODFET structure.

The small-signal a.c. network model was used for the calculations of the power gain versus frequency beyond the unity current gain frequency and the stability gain margin for the same frequency range for submicron gate-length MODFET's. Results of this theoretical investigation evolved into the concept of the high aspect ratio gate electrode design approach to the MODFET structure for millimeter-wave device application, as presented in a paper published in the January 1985 issue of the IEEE Transactions on Electron Devices. (See Appendix I.) A second paper that provides the details of submicron gate-length device design calculations and graphical presentations of the d.c. and a.c. characteristics of MODFET's has also been submitted for publication. (See Reference (a) 4 under Bibliography.) A third paper concerning the scattering parameters of submicron devices based on the overall physical network model is currently under preparation.

The high aspect ratio MODFET's are naturally enhancement mode devices and their limitations as switching devices are of considerable interests. For this reason calculations of power dissipation and propagation delay were carried out for devices

of different sizes, and minimum propagation delay of 10 pSec was predicted for power dissipation of 150 mW for 0.25-μm gate-length devices. (See Reference (b) under Bibliography.)

Experimental Investigation

At the earlier stage of this program the MODFET test devices were not available, and practical investigations could only be pursued involving conventional GaAs MESFET's. The modeling and characterization of the series source and drain resistances was considered to be worthwhile, as the MODFET is known to have similar series resistance limitations. Several short gate-length and long gate-length MESFET's were experimentally investigated for this purpose, and subsequently an analytical model was developed to explain the experimental data. A short communication on our findings was published in the July 1984 issue of IEEE Electron Device Letters. (See Appendix II.) A full paper based on details of our experimental and theoretical results has been submitted to the IEEE Trans. on Electron Devices for publication. (See Reference (a) 2 under Bibliography.)

In early April of 1984, MODFET test samples for mobility and carrier concentration evaluation were supplied by Dr. H. Morkoc. He also provided 1-μm gate-length MODFET test samples for the evaluation of carrier velocity saturation and power gain and noise performance comparison with theoretically predicted performance based on the models developed under this program. The carrier mobility and concentration profile data on the two-dimensional electron gas were obtained experimentally by Dr. D. Look and his associates at 300K and 77K. These data were used in the interpretation of the characteristics of 1-μm gate-length devices, based on the combined charge-control/carrier saturation velocity model, and determination of the carrier saturation velocity parameter as presented in a short paper published in the IEEE Electron Device Letters, November 1984. (See Reference (a) 5 under Bibliography.)

Microwave power gain and noise figure performance were measured using several 1-μm gate-length devices, and the best performances were obtained at a moderate drain current when the transconductance was somewhat below its maximum value. For example at $I_{D\text{-}sat} \simeq 12$ mA and $V_{DS} = 3V$, the noise figure measured was 3.36 dB and the associated power gain was 9.2 dB at 9.36 GHz. These results were quite in line with

the predictions based on the network model developed under the theoretical investigation and were further supported by the s-parameter data obtained from the same test sample.

ACHIEVEMENTS

Planned objectives that were accomplished are listed below:

(a) Identification of the high aspect ratio design approach as the primary means of achieving high power gain with stability in submicron MODFET structures. This provides a solid foundation for millimeter-wave device realization.

(b) Characterization of series resistances in MESFET's and recognition of the effects of free-surface barrier depletion in short gate-length devices.

(c) Determination of the carrier saturation velocity from electrical measurements on 1-μm gate-length MODFET test samples.

(d) Calculations and graphical presentation of submicron gate-length device design parameters and the corresponding small-signal a.c. network model parameters.

(e) Submission of a patent application with two other AFWAL associates that involves the design considerations for depletion-mode mm-wave MODFET's with ohmic and hetero-structure gate constructions. (See Reference (c) under Bibliography.)

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(Accepted for publication in IEEE on Electron Devices)

APPENDIX I (Revised 5/14/84)

A HIGH ASPECT RATIO DESIGN APPROACH TO MILLIMETER-WAVE HEMT STRUCTURES

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ABSTRACT

In MESFET and HEMT structures as the gate-length is reduced below 0.5μm, in an attempt to achieve amplification at highest possible frequencies, it is essential that the depletion depth under the gate be also reduced in order to preserve a high aspect ratio that ensures a high device voltage gain factor (g_m/g_o) and a reasonable value of stable power gain at high frequencies. Results based on this design approach indicate that an (n) AlGaAs/GaAs HEMT structure with 0.25μm gate-length could provide stable power gain in excess of 6dB at the unity current gain frequency of 92.4 GHz, and for an aspect ratio of ten it is difficult to reduce the gate-length below 0.25μm.

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INTRODUCTION

In recent months several research groups have reported interesting results concerning device fabrication technology and microwave performance of sub-micron gate-length MESFET[1-3] and HEMT[4,5] structures. In general, these studies have indicated that while a shortest possible separation between the gate and the source increases the device transconductance, and shortening of the channel length below 0.5μm improves the carrier saturation velocity, they do not necessarily lead to the desired improvement of the device power gain performance. This situation requires a careful optimization approach to design device structures in order to achieve the highest possible power gain with acceptable stability margin. This investigation is an attempt to provide such an optimization approach concerning the HEMT structures.

The structural optimization begins with the recognition of the following facts.

(a) The edge region or the fringing gate-to-drain feedback capacitance (C_{DG}) cannot be reduced beyond a practical minimum that is independent of the depletion depth under the gate.

(b) A sizeable fraction of the source series resistance (r_{SS}) is due to the contact resistance and thus its reduction by lowering the source-to-gate separation is ultimately ineffective.

(c) The magnitude of the stable power gain margin (Y_{21}/Y_{12}) at f_τ is ideally determined by the gate capacitance to the feedback capacitance ratio (C_G/C_{DG}) and in lateral structures this approximates to gate aspect ratio, i.e. the gate-length to the gate depletion depth ratio (L_g/d_o). A high aspect ratio is also desirable in order to obtain a high voltage gain factor (g_m/g_o).

(d) A minimum value of the depletion depth under the gate (d_o) can only be obtained by selecting the highest possible doping concentration.

THE HEMT STRUCTURE

In order to be able to reduce the total depletion depth under the gate, the behavior of the HEMT structure with varying thickness of the n-AlGaAs layer should be understood. Figure 1* depicts a composite schematic band diagram of a Schottky gate heterojunction structure with different n-AlGaAs thicknesses each under a different appropriate forward bias, between the metal gate and the two-dimensional electron gas (2-DEG), via the source ohmic contact, such that the sheet carrier concentration (n_{so}) remains at its maximum value. It is clear from this diagram that for the minimum thickness (d_m) of the high-doped n-AlGaAs layer, required for maximum n_{so}, the forward bias required is same as the magnitude of the Schottky barrier potential, ϕ_B. The value of d_m depends on the doping concentration in the n-AlGaAs layer and to a small extent on the thickness of the AlGaAs spacer layer (d_s). Utilizing the data given in *Delagebeaudeuf and Linh*[6] it has been found that $d_m \approx 70\text{Å}$ and $n_{so} = 1.41\text{X}10^{12}$ cm^{-2} when $d_s = 60\text{Å}$ and $N_D = 2\text{X}10^{18}$ cm^{-3}. Under this condition the potential drop across d_m and d_s are ~74 mV and ~126 mV, respectively. In view of the difficulties in the calculation of these quantities when the doping in the n-AlGaAs is high and the accuracy of the various assumptions involved in the quantum well modeling is in doubt, the exact values of d_m and n_{so} may differ from those given above. Nonetheless based on these values, dimensions of an HEMT structure with 0.25μm gate-length are optimized for best possible performance according to the electrical device model calculations outlined below.

ELECTRICAL CHARACTERISTICS

An important parameter of the HEMT structure is the effective capacitance of the gate that can be related to the sheet carrier concentration in the 2-DEG in terms of the effective gate voltage above its threshold value (V_{TH}).

*Figures located on pgs. I-23 thru I-26.

This capacitance is defined by $(d_m + d_s + d_i)$, where d_m and d_s are as identified above and d_i is the effective distance of the centroid of the 2-DEG from the interface between the undoped AlGaAs and GaAs buffer layers. Approximate value of d_i could be as much[7] as 80A. Thus the value of the per unit area gate capacitance (C_o) can be calculated to be $5.1X10^{-7}$ F/cm^2. Note that the notations used here for different thicknesses differ from those given in ref. (7).

SATURATION CURRENT AND TRANSCONDUCTANCE

The available carrier sheet concentration in the 2-DEG can be controlled by the applied gate voltage (V_{GS}) according to the relationship[6,7]

$$qn_s = C_o (V_{GS}-V_{TH}) \qquad (1)$$

where $$V_{TH} = (\phi_B - \frac{qN_D d_m^2}{2\epsilon} - \Delta\phi c) \qquad (2)$$

and the Fermi level in n-AlGaAs is assumed almost coincident with E_c. For the minimum n-AlGaAs thickness d_m = 70A, when $N_D = 2X10^{18}$ cm^{-3}, $\Delta\phi_c \simeq 320$ mV (the heterojunction discontinuity potential), and $V_{GS} \sim |\phi_B|$, the maximum effective bias voltage ($V_{GS} - V_{TH}$) becomes 400 mV. However, using $n_{so} = 1.41X10^{12}$ cm^{-2} one obtains qn_{so}/C_o 442 mV. Using a lower value of n_{so} reported by Lee et al.[8] this bias becomes 345 mV. Thus there arises the uncertainty as to which value should be taken for calculations. For the calculations reported in this paper maximum effective bias used is 442 mV and other values used are 221 mV and 110.5 mV. Use of 345 mV instead of 442 would reduce the saturation current and the transconductance as given later in Table II, by less than 25% and 2.4%, respectively; the series source and drain resistance would change negligibly because of the contact resistance. The H.F. performance, as

presented later in Table III, would not be significantly affected by the possible difference in the maximum bias voltage cited.

The d.c. and small-signal a.c. parameters values were calculated using the equations[9] given in Table I. The saturation current and transconductance expressions were obtained assuming that the current saturation occurs due to carrier velocity saturation[10,11]. The output conductance (g_o) was not determined theoretically instead assumed values have been used in the present calculations on the basis of experimentally observed behavior of this parameter in short channel devices. For example, in the 0.25μm gate-length devices with 2.1μm and 0.5μm channel g_m/g_o values of 10 and 12.3 respectively have been observed[2]. The saturation carrier velocities in these two channel length cases were $1.1X10^7$ cm/sec and $1.9X10^7$ cm/sec respectively. This apparent increase in the steady state carrier saturation velocity with reducing channel length is caused by the reduction of collisions giving rise to what is known as the ballistic motion[12]. A recent study[13] of high field electron transport in GaAs has revealed that the peak steady state electron velocity can approach $4X10^7$ cm/sec for 0.5μm channel under a uniform field of 10 kV/cm. It is however, difficult to translate this high carrier velocity in an FET channel where the field is highly non-uniform and perhaps for this reason the effective saturation velocity is v_{sat} in a 0.5μm channel[2] is only $1.9X10^7$ cm/sec. The assumed manner in which the carrier mobility depends on the electric field is indicated in the mobility expression given in Table I and this has been used in the present design calculations as others have used previously[11].

The current and transconductance values calculated for the assumed 0.25μm gate-length device with 1mm gate width at specified gate bias conditions are presented in Table II.

Table I. Device Performance Equations and Assumptions

Basic Equations	Assumptions
1. Drain saturation current vs. gate voltage $I_{D\text{-}sat} = g_m\|_{max} V_c(1+ U_G - \sqrt{1 + 2U_G})$ where $U_G = V_G/V_c$ and $g_m\|_{max} = \frac{Z \varepsilon_s v_{sat}}{d_m + d_s + d_i}$	Z: channel width V_G: $(V_{GS} - V_{TH})$ ε_s: semiconductor permittivity $V_c = L_g \mathcal{E}_c$ Lg: gate length $\mathcal{E}_c = v_{sat}/\mu_o$ $\mu = \mu_o/(1 + \mathcal{E}/\mathcal{E}_c)$
2. Transconductance vs. gate voltage $g_m = g_m\|_{max} (1 - \frac{1}{\sqrt{1 + 2V_G/V_c}})$	
3. *Input gate capacitance* $C_G = \frac{\gamma_1 Z \varepsilon_s L_g}{d_m + d_s + d_i}$, $\frac{2}{3} \leq \gamma_1 \leq 1$	γ_1 approaches unity with the increase of velocity saturated carriers.
4. Drain-to-gate feedback capacitance $C_{DG} = Z \varepsilon_s \gamma_2$, $\gamma_2 \cong 1$	γ_2 depends on the location of the saturation point and additional contributions from interelectrode parasitic effects.
5. Drain-to-source output capacitance $C_{DS} = Z\varepsilon_s K(m)/2K(n)$	K: complete elliptic integral of the first kind L_{CH}: channel length $n = L_g/L_{CH}$ $m^2 + n^2 = 1$
Amplifier Performance	
6. Upper-bound of maximum available power gain, $G_{mA}\|_{up} \cong \frac{\theta}{4} (\frac{f_\tau}{f})^2 (\frac{g_m}{g_o})$	$G_{MA}\|_{up} = \frac{(Y_{21})^2}{4\, Re(Y_{11})\, Re(Y_{22})}$ $f_\tau = \frac{g_m}{2\pi C_G}$

Table I (continued)

Basic Equations	Assumptions
where	
$\frac{1}{\theta} = \frac{1}{\eta} + (r_{SS} + r_{GG})\, g_m/\Delta$	$\eta = \frac{1}{g_m r_{CH}}$
$3 \leq \eta \leq 5$	$\Delta = (1 + g_m r_{SS})$
	g_o: output conductance
	r_{SS}: source resistance
	r_{GG}: gate series resistance
7. Upper-bound of maximum oscillation frequency, $f_{max\|up} \simeq f_\tau \sqrt{\frac{\theta}{4}\left(\frac{g_m}{g_o}\right)}$	$g_m >> \omega C_{DG}$
8. Maximum stable power gain margin, $G_{ms} \simeq \left(\frac{f_\tau}{f}\right) \frac{C_G}{C_{DG}} \frac{1}{\Delta} \frac{1}{\gamma_3}$	(see Appendix A.1) $\gamma_3^2 = 1 + \left(\frac{1}{\eta} + \frac{g_m r_{SS}}{\Delta}\right)^2$
9. Actual maximum available power gain, $G_{mA} = \frac{G_{mA\|up}}{1 + \delta_F}$	$\delta_F \simeq \frac{C_{DG}(1 + 2.5C_{DG}/C_G)\,\Delta^3}{5C_G g_o (r_{CH}\Delta + r_{SS} + r_{GG})}$
10. Maximum frequency of oscillations $f_{max} = \frac{f_{max\|up}}{\sqrt{1 + \delta_F}}$	(See Appendix A.2)

PARASITIC CAPACITANCE AND RESISTANCE ELEMENTS

The origins of parasitic capacitance elements are identified in the device cross-sectional schematic shown in Figure 2(a) and an equivalent network representation that includes these elements is shown in Figure 2(b).

The most important of the parasitic capacitances is the drain-to-gate feedback capacitance (C_{DG}). This mainly consists of the sidewall depletion in the n-AlGaAs, a small parasitic coupling between the metal gate edge and the 2-DEG, and another small parasitic component outside of the semiconductor between the metallized gate and drain sidewalls. Under a large operating drain voltage the semiconductor depletion sidewall capacitance will tend to decrease. A detailed calculation[14] of this capacitance is difficult, however an approximate realistic value can be obtained considering that this is equivalent to the edge region fringing capacitance between a parallel plate capacitor with the lower plate (channel) extending indefinitely beyond the edge of the upper plate (gate). This is almost independent of the separation between the parallel plates as indicated in Table I. This capacitance can be represented in two parts, one being the inner component and the other the outer component (see Figure 2(a)). The total value of C_{DG} for a 0.25μm drain/gate separation can have a maximum value of 0.203pF/mm and a minimum value of 0.155pF/mm depending on the drain bias voltage. Included in this is the capacitance between the metallization sidewalls (~0.035pF/mm).

The source-to-gate capacitance (C_{SG}) has a similar origin as that of C_{DG} and due to a lower gate/source voltage its value would be larger than that of C_{DG}. In a device with a minimum depletion depth (~210A) and a gate-length of 0.25μm, the gate capacitance C_G becomes much larger than C_{SG} and for this reason an exact knowledge of the latter is unimportant.

The source-to-drain parasitic capacitance (C_{DS}) can be modeled[8] by assuming that this is equivalent to the one-sided capacitance between two conducting co-planar stripes separated by a small gap[15]. This will be distributed between the drain and source resistances. For 0.25μm gate-length and 0.75μm channel length this capacitance becomes ~0.084pF/mm. There is another inner component of C_{DS} due to the distributed channel resistance under the gate and its coupling with the drain conducting region via the buffer layer (see Figure 2(b). This capacitance could be as much as the outer component of C_{DS} cited above.

There are three resistances that can be presented in series with the terminals of the FET structure. The most important of these is the source series resistance (r_{SS}); it consists of two parts - one arises due to the contact resistance (ρ_c) and the other is due to the ungated channel between the source and the gate. Assuming $n_{so} \simeq 1.41X10^{12}$ cm^{-2} and a mobility value of $8X10^3$ $cm^2/Vsec$, one obtains 0.235Ωmm for the contact related part of r_{SS} when $\rho_c = 10^{-6}\Omega cm^2$. Assuming a source/gate separation of 0.25μm one obtains 0.083Ωmm for the ungated part of r_{SS} for the same mobility and sheet carrier concentration values. This would imply that r_{SS} can have a value of ~0.32Ωmm. This is quite in line with the reported[4] value of ~1.27Ωmm for a gate/source gap of 0.7μm. For the determination of the drain series resistance (r_{DD}) a similar approach can be used and usually its value can be somewhat higher than r_{SS} due to a higher gate/drain separation. However, too high a separation in sub-half-micron gate could be deleterious to obtaining a high carrier saturation velocity.

The series resistance of the gate metallization is usually lowered by parallel gate pad arrangement such that only small fraction of the entire gate width (Z) is encountered in signal flow-path. For millimeter-wave devices

this fractional gatewidth should remain below 50μm so that lumped network element modeling concept is not invalidated. By a careful arrangement of the gate metallization, Chao, et al.[4] have demonstrated that for 150μm gate width for 0.25μm gate-length a gate resistance (r_{GG}) value of 0.8Ω is possible. An extrapolation based on this value with multiple gate pad arrangement should give r_{GG} below 0.1Ω for a total gate width of 1 mm. In discrete devices wirebonding and distributed gate pattern would require an appropriate representation by suitable inductive elements in series with the gate, source and drain terminals. However, in integrated circuits their effects can be minimized or absorbed in passive circuit-elements by a careful chip layout procedure. In this work these inductances are considered to be absent.

POWER GAINS AND AMPLIFIER STABILITY

Depletion mode high electron mobility FET structures were analyzed[16] for power gain and stability performance, based on n-AlGaAs doping concentration of ~$7X10^{17}cm^{-3}$ and gate-lengths of 1, 0.5 and 0.25μm with different channel lengths, using the detailed form of the equivalent network model (see Figure 2(b)) following the standard circuit analysis approach.[17] Due to the large values of the parasitic resistance and capacitance elements and comparatively low values of the gate capacitance no useful simplification of the power gain expressions could be made and the calculated data indicated that although there is potential power gain in some cases the stability margins in all cases were too small for practical use. However, when the parasitic capacitance values are much lower than the active gate capacitance magnitude, and the associated parasitic RC time constant values are much smaller than the effective channel carrier transit time then the power gain expressions can be

simplified as given in eqns. 6, 7 and 8 of Table I. It is particularly instructive to note how a high $g_m r_{ss}$ product can reduce the upper-bound of the power gain by 6 to 8 dB depending on the value of η, and also its influence on the stable power gain margin. The basis for the derivation[18] of the upper-bound of the power gain is given in Appendix A.1.

In the case when the drain-to-gate feedback capacitance is not negligible comparable to the gate capacitance, the actual power gain can become lower than its upper-bound value. Approximate results representing this situation are also given in eqns. 9 and 10 in Table I, and the relevant analytical steps are given in Appendix A.2. For the purpose of numerical determination of various power gains versus frequency behavior of a 0.25μm gate-length device with a high aspect ratio, all structural dimensions and relevant electrical parameter values are listed in Table II. The results showing the upper-bound of power gain performance are given in Table III(a).

Prediction of realistic values of f_{max} and power gain at f_τ would be of great interest to those who are currently involved in the R and D activities concerning HEMT structures. For this reason calculations based on the equations obtained in this paper and reported by others[19,20] are compared in Table III(b) for the selected device structure. The equation for f_{max} obtained by Wolf[19] can be recast in the following manner,

$$f_{max} \simeq \frac{f_\tau}{\sqrt{4g_o(R_{CH} + r_{SS} + r_{GG}) + \frac{2C_{DG}}{C_G}\left\{\frac{C_{DG}}{C_G} + g_m (R_{CH} + r_{SS})\right\}}} \qquad (3)$$

For comparison purposes the f_{max} equation given in Table I (eqn.10) can also be rearranged in the same fashion, as given below:

$$f_{max} = \frac{f_\tau}{\sqrt{4g_o\left(R_{CH} + \frac{r_{SS} + r_{GG}}{\Delta}\right) + \frac{4}{5}\,\frac{C_{DG}}{C_G}\left(1 + \frac{2.5C_{DG}}{C_G}\right)\Delta^2}} \qquad (4)$$

TABLE II: PHYSICAL AND ELECTRICAL PARAMETERS (300K)

(a) Calculated parameters vs. gate bias voltage

$(V_{GS}-V_{TH})$	I_{D-sat}	g_m	$1/g_m$	η	r_{CH}	γ_1	C_G	C_G/C_{DG}	f_τ	$\tau = C_G/g_m$
mV	mA/mm	mS/mm	Ω.mm	-	Ω.mm	-	pF/mm	-	GHz	psec
442	256.2	725.1	1.379	3	0.4596	0.98	1.248	8.05	92.4	1.72
221	104.5	638.8	1.575	3.5	0.4500	0.95	1.210	7.80	83.4	1.91
110.5	39.6	523.3	1.911	4.5	0.4244	0.90	1.146	7.39	71.6	2.22

(b) Assumed parameters

$d_m = 70\text{Å}$ $\quad \mu_o = 8\text{X}10^3\ cm^2/\text{Vsec}$ $\quad \rho_c = 10^{-6}\ \Omega\text{-cm}^2$

$d_i = 80\text{Å}$ $\quad \varepsilon = 1.07\text{X}10^{-12}\ F/cm$ $\quad r_{GG} = 0.1\Omega$

$d_s = 60\text{Å}$ $\quad v_{sat} = 1.9\text{X}10^7\ cm/sec$ $\quad$ (for Z = 0.1cm)

$L_g = 0.25\mu m$ $\quad \Delta\phi_c = 320\ mV$ $\quad r_{DG} = 0$

$L_{CH} = 0.75\mu m$ $\quad n_{so} = 1.41\text{X}10^{12}cm^{-2}$ $\quad g_m/g_o = 10$

Z = 0.1 cm

$C_{SG} \ll C_G$

(c) Calculated fixed parameters:

$\rho_s = 555\ \Omega/\text{square}$ $\quad g_{m/max} = 968\ mS/mm$

$\mathcal{E}_c = 2.375\text{X}10^3\ V/cm$ $\quad r_{SS} = 0.32\ \Omega.mm$

$V_c = 59.3\ mV$ $\quad r_{DD} = 0.32\ \Omega.mm$

$V_{TH} \simeq 500\ mV$ $\quad c_{DG} = 0.155pF/mm.$

TABLE III. (a). BIAS DEPENDENCE OF UPPER-BOUND PERFORMANCE

$I_{D\text{-sat}}$ mA/mm	f_τ GHz	$G_{MA/UP}$ at f	G_{MS} at f	$f_{max/UP}$ GHz
256.2	92.4	6.33dB	6.67dB	191
104.5	83.4	6.93dB	6.70dB	185
39.6	71.6	7.84dB	7.15dB	176

(b) COMPARISON OF ACTUAL PERFORMANCE WHEN f_τ = 92.4 GHz

Performance	(Wolf)[19]	(This work)	(Curtice)[20]
f_{max}(GHz)	138.5	141	154
G_{mA} (dB) (at f_τ)	3.54	3.73	4.46

where

$$\Delta = (1 + g_g r_{SS})$$

There are differences in these two equations and reason is that Wolf[19] ignored the source feedback term $g_m r_{ss}$, and his estimation of the imaginary part of y_{21} was also different (see Appendix A.2). Nevertheless, the closeness of results calculated from these equations are quite remarkable in the specific case considered. The equation reported by Curtice[20] gives the highest value since he introduced a negative term under the square root sign in eqn.(3) that includes the effect of the inner part of C_{DS} as shown in Figure 2.

The significance and importance of the proposed high gate aspect ratio design can be best appreciated by focussing on the ratio C_{DG}/C_G in eqn.(8) of Table I and in eqn.(4). In the former, at f_τ and beyond the stability is seen to be directly proportional to the aspect ratio (see also eqns. 3 and 4 in Table I). In the latter, the aspect ratio should be high for the realization of the upper-bound of performance.

DEVICE REALIZATION

Manufacturing of high aspect ratio enhancement-mode HEMT's would require careful control of the thickness and doping concentration in the n-AlGaAs layer and its protection from the effect of free-surface potential in the gate-to-drain and gate-to-source separation regions. A structure that would achieve these objectives is schematically shown in Figure 3. In the gate region the capping n-GaAs layer is removed by etching utilizing the differential etching properties[5] of AlGaAs and GaAs. The thickness of this layer is predetermined and grown by MBE technique. A typical combination of doping and thickness values are indicated in Figure 3. For approximately zero threshold voltage and complete depletion of the n-AlGaAs layer, under the maximum

allowed positive gate bias voltage, the relevant band and field diagrams are shown in Figure 4. The extent of the total gate voltage swing is indicated by the hatched area, plus that due to d_i.

Note that the gate metal not only forms Schottky barrier at the n-AlGaAs interface, the same is also formed at the n-GaAs sidewalls. This provides complete electrical isolation due to depletion and for this reason the n-GaAs layer doping should be not too high. Within the interelectrode spacing n-AlGaAs also provides 2-DEG to the n-GaAs and this should have no undesirable effects on the device performance. The free-surface potential should only affect the n-GaAs surface and thus protect the thin active n-AlGaAs layer and this could enhance the device reliability.

For convenience the gate metallization can be achieved by a technique similar to that employed in the self-aligned gate technique[3] involving refractory metals. This would permit alloying of the source and the drain ohmic contacts after the gate is defined. The gate aspect ratio in the suggested device structure could easily exceed ten for a gate-length of 0.25μm as required for the desired millimeter-wave performance.

DISCUSSIONS AND CONCLUSIONS

The calculated power gain performance, based on device parameter values, in line with what have been reported in the literature, clearly demonstrate the feasibility of achieving millimeter-wave HEMT structure that would operate in enhancement mode. It is perhaps not unrealistic to extrapolate this to MESFET structures, too. For practical realization of very thin depletion depth under the gate electrode it might even be appropriate to increase the doping concentration to $4X10^{18}cm^{-3}$. The need to reduce the source series resistance is there, however, an order of magnitude reduction of the contact resistivity will be required to reduce r_{SS} by a factor of two. The parameters

that have the most influence on the power gain performance are the carrier saturating velocity (through f_τ) and the voltage gain factor (g_m/g_o), assuming that the gate aspect ratio has already been fixed due to practical limitation. Since v_{sat} and g_o both increase with the reduction of channel length, no easy compromises are possible to achieve high power gains at higher and higher frequencies. To improve the situation in sub-half-micron structures, reduction of g_o by incorporation[21] of a carefully buried p^+/n^+ region below the active channel, that would naturally be fully depleted, should be considered.

The predicted upper-bound values of the maximum frequency of oscillations (191GHz) and the power gain (6.33 dB) at 92.4 GHz are encouraging figures for future development and research. However, for the aspect ratio used, the feedback capacitance is still appreciable compared to the gate capacitance and this reduces the f_{max} and power gain at 92.4 GHz considerably as given in Table III(b). It is believed that by further increasing the aspect ratio, by reducing spacer layer and/or the n-AlGaAs layer thickness (by increasing doping), the actual performance may be pushed towards the upper-bound values of the structure. Reduction of contact resistance would also be helpful.

In view of the imprecise values of v_{sat} and g_o, at the present state of understanding of device physical processes, it is not possible to predict exactly as to how high in frequency the device performance can be extended. Nevertheless, aided by the proposed high gate aspect ratio design approach, it should be possible to obtain reasonable millimeter-wave amplifying performance from a 0.25μm gate HEMT Structure. This being an enhancement HEMT its usefulness in high speed switching circuits need not be further emphasized.

ACKNOWLEDGMENTS

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Appendix A

A.1 The Basis for $G_{mA/up}$ Expression

The network model of Fig. 2(b) can be used to define Y'-parameters that includes the effects of r_{SS} and then the overall Y-parameters can be calculated by including the effects of r_{GG}. Following this approach the upper-bound of the maximum available power gain can be approximated to

$$\frac{1}{4}\frac{|Y_{21}|^2}{Re(Y_{11})Re(Y_{22})} \simeq \frac{|Y'_{21}|^2}{4\omega^2 C'^2_G (r'_{CH} + r_{GG})\, g'_o} \tag{1}$$

where $r'_{CH} = \frac{\Delta}{\eta g_m} + r_{SS}$; $g'_o = g_o/\Delta$

$C'_G = C_G/\Delta$; $\Delta = 1 + g_m r_{SS}$

and $|Y'_{21}| \approx g_m/\Delta$

These approximations are valid when r_{GG} is low, c_{DG} is much smaller than C_G and $\omega^2 C_{DG}^2 (r_{DD}/g'_o) << 1$, as would be the case for high aspect ratio designs. A final form of eqn.(1) above is given in Table I eqn.(6).

A.2 The Effect of C_{DG} on the Power Gain

In practice C_G/C_{DG} ratio may be less than 10, and this could have noticeable effect on the actual power gain. This effect can be calculated by not neglecting the Re $(Y_{12}\, Y_{21})$ term in the stability factor given by,

$$K = \frac{2Re(Y_{11})Re(Y_{22}) - Re(Y_{12}Y_{21})}{|Y_{12}\, Y_{21}|} \tag{2}$$

when $K \geq 2$, which is usually true above f_τ, the actual gain can be written as

$$G_{mA/up} = \frac{G_{mA/up}}{1 + \delta_F} \tag{3}$$

$$\text{where } \delta_F = \frac{-Re(Y_{21}Y_{22})}{2\, Re(Y_{11})Re(Y_{22})}$$

In reference (18), the intrinsic Y^i_{21} parameter is given by,

$$Y^i_{21} \simeq \frac{g_m \exp(-k_{cof}/sf_\tau)}{1 + jf/sf_\tau} \tag{4}$$

where $s \simeq 4$ and $k_{co} \simeq 0.61$, similar to those for MOSFET's[22,23]. For frequencies below $2f_\tau$, the imaginary part of Y_{21}^i as given in eqn.(4) and the same quantity as may be obtained from the intrinsic part of the network model in Fig. 2(b) can be shown to become, $-j\omega C_G(k_{co}+1)/s$ and $-j\omega C_G/\eta$, respectively. This difference arises due to the network representation of g_m with reference to the signal voltage across the gate capacitance. However, the magnitude $|Y_{21}|$ remains nearly the same in both representations. Thus for greater accuracy, we have taken

$$\mathrm{Im}(Y_{21}^i) \simeq -j \frac{\omega C_G}{2.5} \tag{5}$$

The value of the delay factor k_{co} in eqn.(4) can be increased to represent additional delay that takes place in the velocity saturated region near the drain and in that case the factor 2.5 should be appropriately reduced. Thus from above we have

$$\mathrm{Re}\,(Y_{12}Y_{21}) \simeq -\omega^2 C_{DG}\,(C_{DG} + \frac{C_G}{2.5}) \tag{6}$$

and for the product $\mathrm{Re}(Y_{22})\mathrm{Re}(Y_{11})$, the approximate form in the denominator of eqn.(1) above can be used. Finally, the expression of G_{mA} and f_{max}, as given in Table I, can be obtained.

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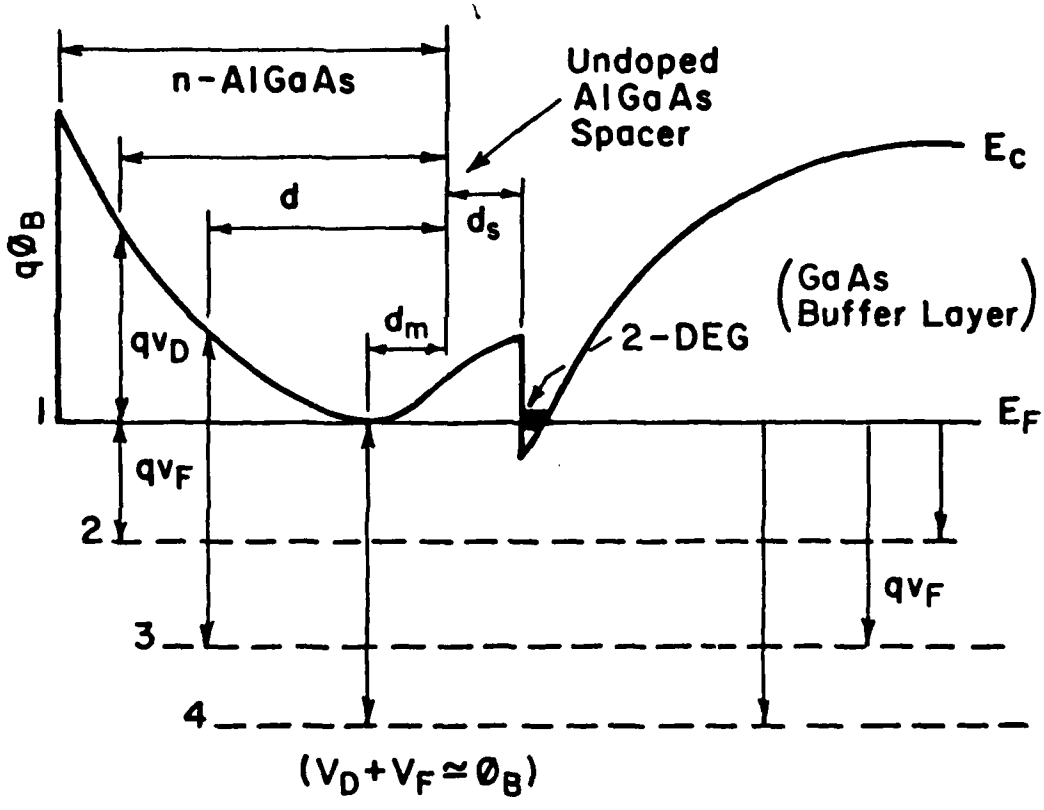
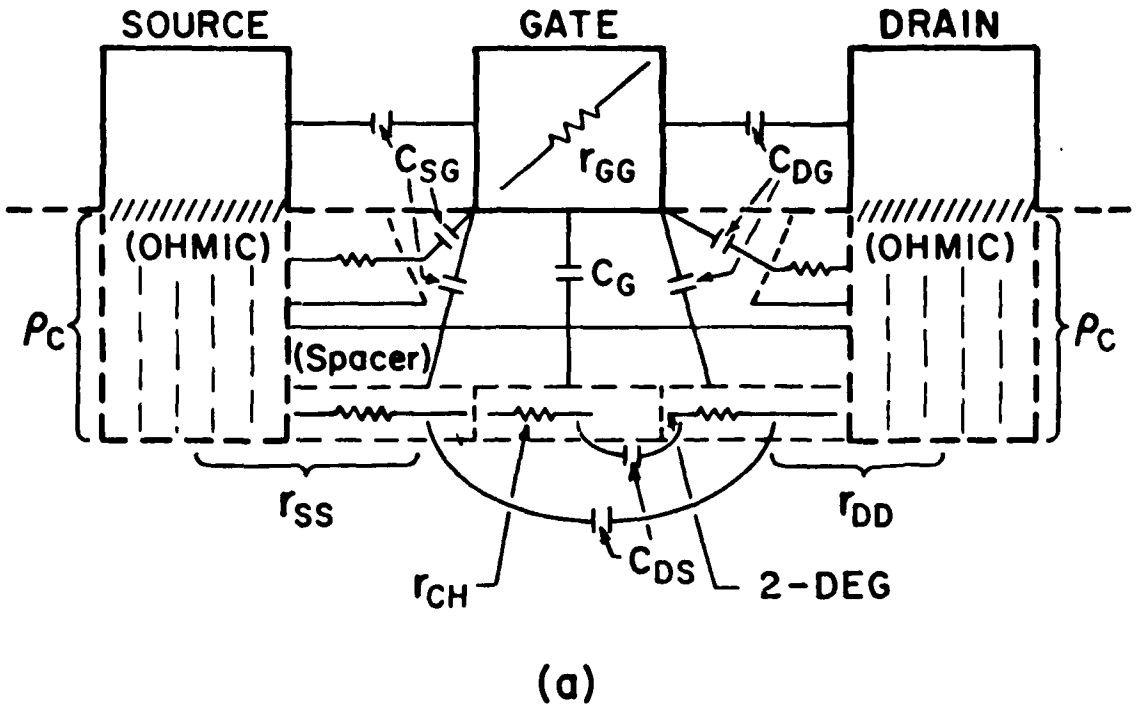


Figure 1. The effects of n-AlGaAs layer thickness variation on the magnitude of the forward bias required to obtain the same value of n_{so}.



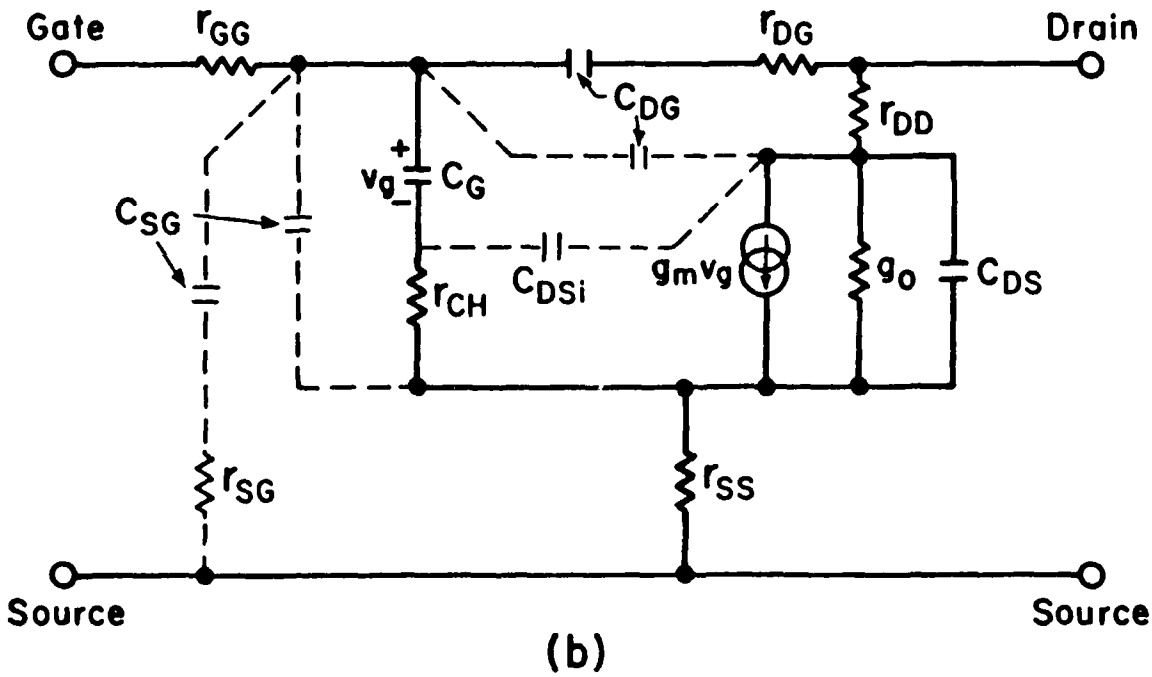


Figure 2. (a) Cross-sectional schematic of a HEMT structure, and its (b) lumped equivalent network representation. (Circuit elements shown by dotted lines are of less significance.)

A HIGH-ASPECT-RATIO S.B.-GATE ENHANCEMENT-MODE HEMT STRUCTURE

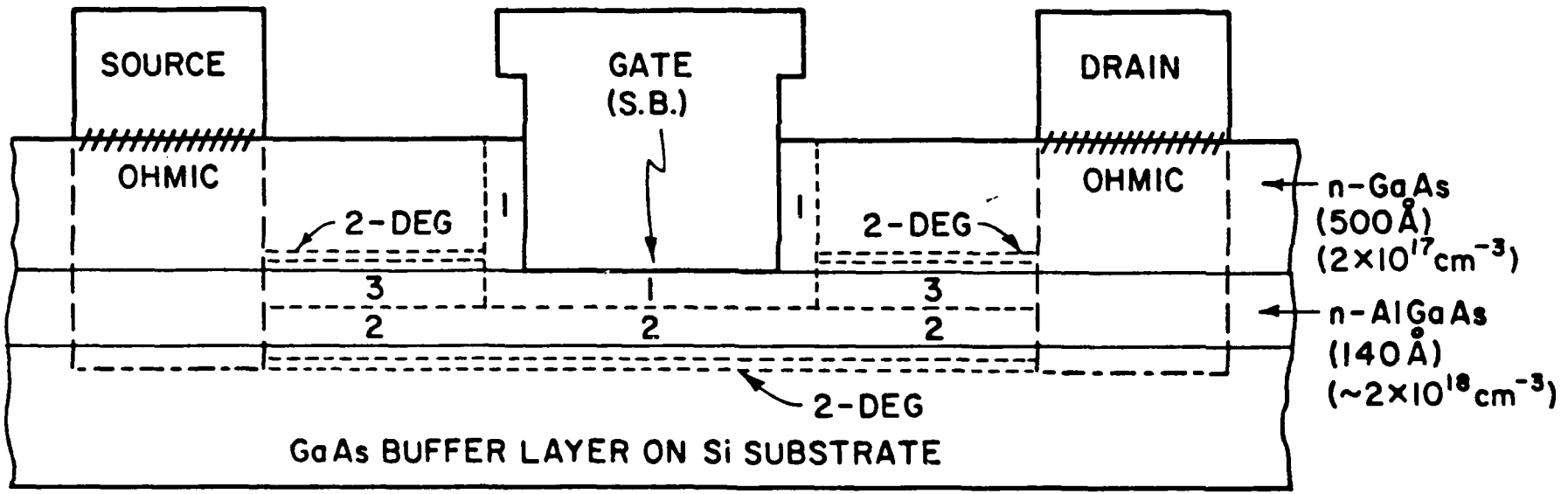


Figure 3. Cross-sectional schematic of a proposed high aspect ratio enhancement-mode HEMT structure.

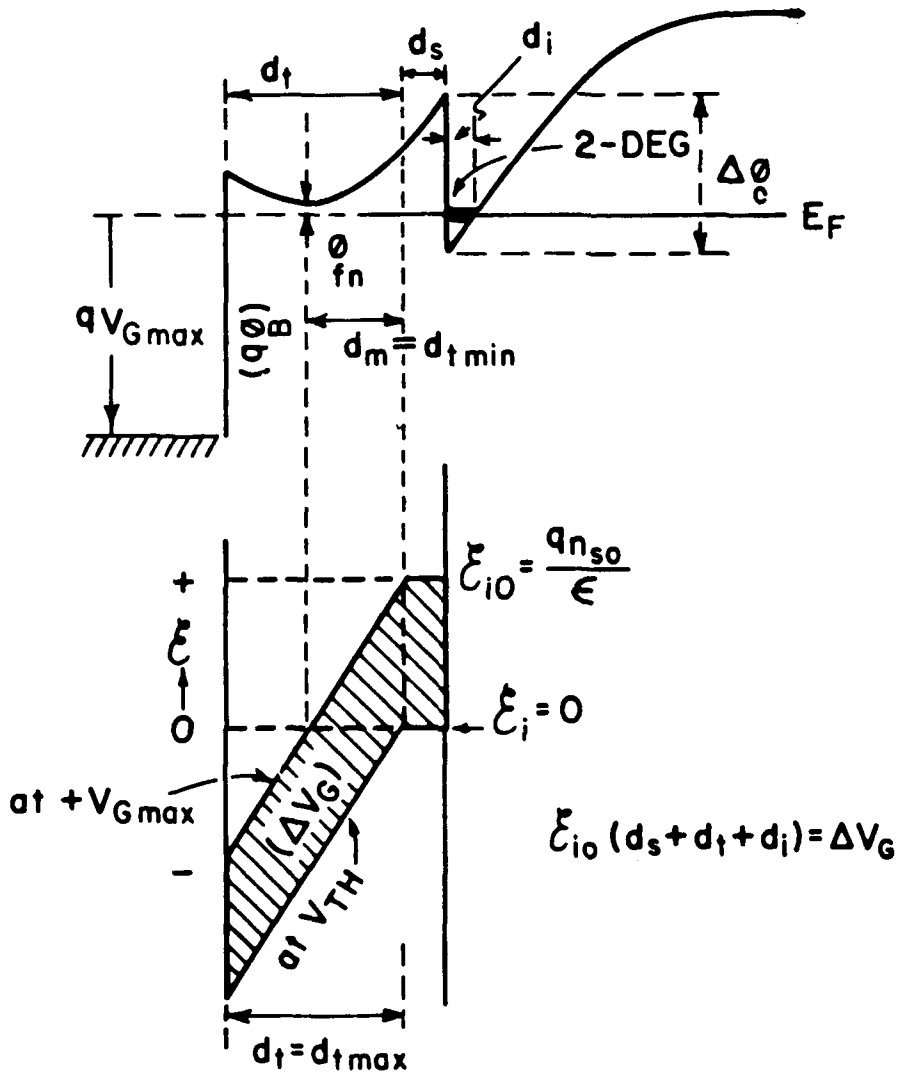


Figure 4. Band and field diagrams for an E-HEMT showing the basis of its operation and voltage swing limitation.

244 IEEE ELECTRON DEVICE LETTERS, VOL. EDL-5, NO. 7, JULY 1984

On the Determination of Source and Drain Series Resistances of MESFET's

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Abstract—**Based on an implicit analytic solution of current transport equations applicable to a forward-biased Schottky barrier or junction-gate FET's with open drain, universal curves for three α-factors have been generated. These factors determine the channel resistance contributions to the device terminal dc and ac resistances. By measuring these resistances the values of the channel, source, and drain resistances have been determined.**

USING an approximate solution to the current transport equations, under the conditions of forward-biased gate and floating drain (see Fig. 1), Lee *et al.* [1] have shown that the open-circuit drain voltage to the gate current ratio is a measure of the "end" resistance [2] that is interpreted as the sum of one-half of the channel resistance and the extrinsic source resistance (R_{ss}). In order to determine the value of R_{SS} and R_{DD} (drain resistance) they have suggested to combine these data with a plot of the measured source-to-drain resistance against the calculated values of the channel sheet resistance, corresponding to different gate bias voltages, and thus obtain the sum of R_{SS} and R_{DD} by extrapolation and hence R_{SS} and R_{DD}. This approach requires a prior knowledge of the channel sheet resistance versus gate voltage behavior. Also the solution obtained by them is based on the assumption that the channel voltage drop is much less than $\eta kT/q$, where η is the diode factor and kT/q is the thermal potential. However, this can be readily violated in practice.

We have obtained an implicit closed-form solution to the same set of differential equations without any restrictions to the channel voltage drop. This solution has enabled us to define three α-factors by which the channel resistance (R_{CH}) under the gate should be multiplied if the resistances are measured under different conditions as indicated below.

The floating drain voltage-to-gate current ratio is as follows:

$$R_f = \frac{V_{DS}}{I_g} = R_{SS} + \alpha_D R_{CH}. \tag{1}$$

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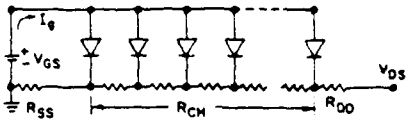

Fig. 1. Schematic representation of the forward-biased MESFET with floating drain.

The small-signal transfer resistance is given by

$$r_t = \frac{\partial V_{DS}}{\partial I_g} = R_{SS} + \alpha_t R_{CH}. \tag{2}$$

The small-signal input resistance is

$$r_{in} = \frac{\partial V_{GS}}{\partial I_g} = r_i + \frac{\eta kT}{qI_g} \tag{3}$$

where

$$r_i = R_{SS} + \alpha_i R_{CH} \tag{4}$$

and I_g is the gate current and V_{DS} and V_{GS} are the drain-to-source and gate-to-source voltages, respectively.

The above three α-factors are graphically presented in Fig. 2, against the normalized gate current. Note that the effective thermal potential $\eta kT/q$ and the channel resistance R_{CH} define the normalizing current I_T. It should be emphasized that these curves are universal and the limiting value of α_D is 1/2 at low currents, as obtained by Lee *et al.* [1]. The low current values of α_t and α_i are 1/2 and 1/3, respectively. This low current value of α_i can be readily obtained by taking the limiting value of the driving point impedance (z_{in}) of the conductance (diode)/resistance (channel) distributed network [3] as given in Fig. 1. Namely,

$$z_{in} = \sqrt{r_{CH}/g_D}\coth\sqrt{r_{CH}g_D L^2} \approx \frac{1}{g_D L} + \frac{1}{3} r_{CH} L \tag{5}$$

where g_D is the diode conductance per unit length, r_{CH} is the channel resistance per unit length, and L is the channel length. Assuming that the diode resistance ($\eta kT/qI_g$) is known, the difference between r_t and r_i readily gives $R_{CH}/6$ at low currents. Once a value of R_{CH} is obtained, improved values of α_t and α_i can be found from Fig. 2 by identifying an appropriate value of I_g/I_T. This will provide an improved value of R_{CH}. This process can be repeated until a steady value of R_{CH} is obtained.

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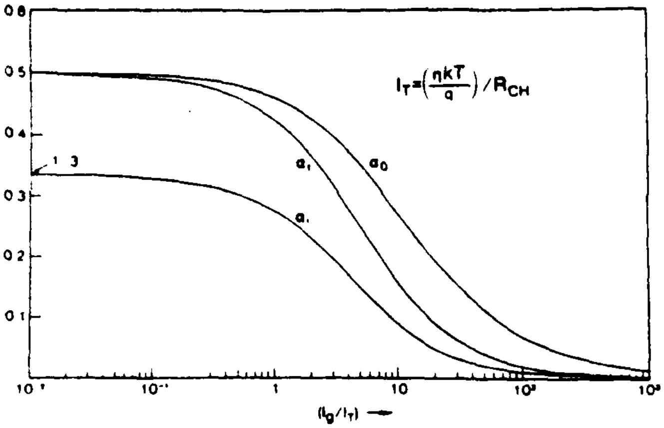

Fig. 2. Universal curves for α_D, α_t, and α_i versus normalized gate current.

Here we present the summary of our preliminary results that were obtained from p-n junction diode/resistance analog to demonstrate the validity of the theoretical model and its application to the determination of the series resistances of a 1-μm gate-length MESFET. The details of the theory and experimental data on different gate-length MESFET's will be published elsewhere. The diode/resistance analog consisted of 11 p-n-junction diodes and ten resistors of equal value. Two sets of resistors were used—one had a value of 5.1 Ω each and the other 27 Ω each. They provided the channel resistance values of 51 and 270 Ω, respectively. The diodes were selected at a constant forward current of 0.5 mA within the forward-bias voltage range of 600 ± 6 mV. The resistors were of a tolerance of ±5 percent. The ideality factor of the diodes was very close to 1 and the thermal potential value was 25.6 mV at room temperature. The measured and calculated values of V_{DS}/I_g, r_t, and r_i, as obtained from the analog networks, after allowing for $R_{SS} \sim 22$ Ω, are presented in Table I. For both values of R_{CH}, the values of r_t, given in the middle column, as measured, agree quite well with those calculated. The measured values of V_{DS}/I_g on all currents appear to be slightly higher than that predicted by the theory. The measured values of r_i appear to be somewhat lower than the calculated values, particularly at high currents. These discrepancies could have been due to the mismatching of the diode I–V characteristics and the resistor elements, as pointed out earlier. Therefore, accepting these expected range of variations and some measurement errors, we can conclude that the theoretical results presented here for the current dependent parameters α_D, α_t, and α_i are indeed valid.

Measurements were also carried out on a 1-μm gate-length microwave MESFET under forward-bias condition for the purpose of determining approximate values of the intrinsic channel resistance (R_{CH}) and the extrinsic source resistance R_{SS} neglecting any gate series resistance. The sample was mounted with grounded source on a microwave stripline module that could readily be adopted to microwave measurement setups. Thus the measurements could only be done to determine R_{SS} and R_{CH} and not R_{DD}. Results of these measurements are presented in Table II. It is important to note that the diode small-signal resistance ($\eta kT/qI_g$) is a large component of the measured input resistance (r_{in}). Thus only results at $I_g \geqslant 0.25$ mA is meaningful for the extraction of r_i and hence the determination of R_{CH} and R_{SS}. By graphical presentation of r_{in} against I_g, an asymptotic representation of the diode resistance can be made that should also reveal the value of η. By increasing the gate current above 1 mA, we observed noticeable thermal effect on the measured data. Since the measurements could not be done rapidly due to possible damage to the device, we restricted our data anlaysis within a limited current range as indicated in Table II. All the ac measurements were performed with an ac gate-to-source voltage of 6 mV at a signal frequency of 25 kHz.

TABLE I
MEASURED DATA ON p-n-JUNCTION DIODE/RESISTANCE ANALOG NETWORKS

R_{CH}	$\frac{I_g}{I_T}$	$\alpha_D R_{CH}$ (ohms)		$\alpha_t R_{CH}$ (ohms)		$\alpha_i R_{CH}$ (ohms)	
		Measured	Calculated	Measured	Calculated	Measured	Calculated
270 ohms	[illegible]	168	[illegible]32.3	[illegible]	[illegible]	-	-
	[illegible]735	155	128.[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
	[illegible]	148	124.[illegible]	122.5	[illegible]	39	[illegible]
	[illegible]	120.5	115.[illegible]	81.8	97.[illegible]	28.[illegible]	[illegible]
	5.25	112	93.1	53.0	66.2	25.6	[illegible]
	[illegible]	91	[illegible]	29.[illegible]	[illegible]	[illegible]	[illegible]
51 ohms	0.4	32	26.5	26.8	[illegible]	-	-
	0.8	35	24.0	19.9	[illegible]	[illegible]	[illegible]
	1.2	33	23.[illegible]	21.[illegible]	21.[illegible]	11	[illegible]
	1.6	30	22.[illegible]	19.5	19.9	10.5	[illegible]
	2.0	28.5	21.[illegible]	19.[illegible]	18.6	[illegible]	[illegible]
	4.0	28	18.3	11.9	[illegible]	-	[illegible]

I_T = 0.[illegible] mA when R_{CH} = 51 Ω

I_T = 0.[illegible] mA when R_{CH} = 270 Ω

TABLE II
MEASURED DATA ON A 1-μm GATE-LENGTH MESFET

I_g	$\frac{V_{DS}}{I_g}$	r_t	r_{in}	$\frac{\eta kT}{qI_g}$	r_i	[illegible]
mA	-	-	-	-	-	-
0.25	[illegible]	[illegible]	[illegible]	130	[illegible]	[illegible]
0.50	[illegible]	11.9[illegible]	75.[illegible]	67	8.[illegible]	3.[illegible]
1.00	12.[illegible]	11.9[illegible]	43.0	34	9.0	[illegible]

$\eta \approx$ [illegible], R_{CH} = 18.[illegible] Ω and R_{SS} = 3.3[illegible] Ω

The values of R_{CH} and R_{SS} were determined utilizing the α_t and α_i curves of Fig. 1. A separate resistance measurement between the source and the drain with the gate shorted to the source indicated an approximate total resistance of 29.5 Ω. This value appears to be quite consistent with the estimated values of $R_{CH} = 18.7$ Ω and $R_{SS} = 3.34$ Ω, together with an appropriate value of R_{DD} that can be expected to be higher than R_{SS}.

In conclusion, we have identified and calculated three current dependent resistances that arise due to the channel resist-

ance of a MESFET when its gate is forward biased with respect to the source and an open-circuit is maintained at the drain. We have also demonstrated that by measuring these resistances at different currents and by using the theoretical curves, channel resistance, series source, and drain resistances of MESFET's can be readily determined.

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